Applied Physics Letters

RESEARCH ARTICLE | APRIL 10 2024

Reduced temperature in lateral $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterojunction field effect transistor capped with nanocrystalline diamond

Hannah N. Masten ; James Spencer Lundh ; Tatyana I. Feygelson ; Kohei Sasaki ; Zhe Cheng ; Joseph A. Spencer ; Pai-Ying Liao ; Jennifer K. Hite ; Daniel J. Pennachio ; Alan G. Jacobs ; Michael A. Mastro ; Boris N. Feigelson ; Akito Kuramata ; Peide Ye ; Samuel Graham ; Bradford B. Pate ; Karl D. Hobart ; Travis J. Anderson ; Marko J. Tadjer

Appl. Phys. Lett. 124, 153502 (2024)
https://doi.org/10.1063/5.0191771

AIP Publishing

Applied Physics Letters ARTICLE pubs.aip.org/aip/apl

Reduced temperature in lateral $(Al_xGa_{1-x})_2O_3$/Ga_2O_3 heterojunction field effect transistor capped with nanocrystalline diamond

Cite as: Appl. Phys. Lett. **124**, 153502 (2024); doi: 10.1063/5.0191771
Submitted: 15 December 2023 · Accepted: 29 March 2024 ·
Published Online: 10 April 2024

View Online Export Citation CrossMark

Hannah N. Masten,[1,a] James Spencer Lundh,[1] Tatyana I. Feygelson,[2] Kohei Sasaki,[3] Zhe Cheng,[4] Joseph A. Spencer,[2,5] Pai-Ying Liao,[6] Jennifer K. Hite,[2] Daniel J. Pennachio,[2] Alan G. Jacobs,[2] Michael A. Mastro,[2] Boris N. Feigelson,[2] Akito Kuramata,[3] Peide Ye,[6] Samuel Graham,[7] Bradford B. Pate,[2] Karl D. Hobart,[2] Travis J. Anderson,[2] and Marko J. Tadjer[2]

AFFILIATIONS

[1]National Research Council, Washington, District of Columbia 20375, USA
[2]US Naval Research Laboratory, Washington, District of Columbia 20375, USA
[3]Novel Crystal Technology, Sayama-city, Saitama, Japan
[4]University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, USA
[5]Virginia Polytechnic Institute and State University, Blacksburg, Virginia 24061, USA
[6]Purdue University, West Lafayette, Indiana 47907, USA
[7]University of Maryland, College Park, Maryland 20742, USA

[a]**Author to whom correspondence should be addressed:** Hannah.n.masten.ctr@us.navy.mil

ABSTRACT

The low thermal conductivity of β-Ga_2O_3 is a significant concern for maximizing the potential of this ultra-wide bandgap semiconductor as a power switching device technology. Here, we report on the use of nanocrystalline diamond (NCD) deposited via microwave plasma enhanced chemical vapor deposition (MP-CVD) as a top-side, device-level thermal management solution on a lateral β-Ga_2O_3 transistor. NCD was grown via MP-CVD on β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 heterostructures prior to the gate formation of the field-effect transistor. A reduced growth temperature of 400 °C and a SiN_x barrier layer were used to protect the oxide semiconductors from etching in the MP-CVD H_2 plasma environment. Raman spectroscopy showed a highly sp^3-bonded NCD film was obtained at 400 °C, with grain size of about 50–100 nm imaged via atomic force microscopy. The incorporation of the NCD heat-spreading layer resulted in a β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 heterostructure field-effect transistor showing a decrease in the total thermal resistance at the gate by 42%. The fabrication process, including the NCD etch in the gate region, will need to be improved to minimize the impact of these processes on important device characteristics (i.e., drain current, threshold voltage, and leakage current).

Significant progress has been made over the years in power devices based on the ultra-wide bandgap semiconductor, β-gallium oxide (β-Ga_2O_3). This material attracts attention due to its excellent electrical properties, including its ultra-wide bandgap E_G of 4.6–4.9 eV and high critical field strength E_c of 6–8 MV/cm, and because of the availability of large-area high-quality single crystalline bulk substrates and epiwafers.[1–3] Even though all semiconductor devices are thermally limited, β-Ga_2O_3 exhibits the lowest thermal conductivity of all relevant semiconductors [highest of 27 W (m K)$^{-1}$ in [010] direction[2,3]] considered for electronic device applications. The expectation of very high power densities resulting from the high E_g of Ga_2O_3 necessitates that a heat extraction mechanism from the active region be implemented. Otherwise, considerable device self-heating will lead to premature device failure.[4–7] β-Ga_2O_3 device reports over the past decade have not addressed this issue yet.

The development of high-performance β-Ga_2O_3-based lateral power devices will require the incorporation of thermal management solutions near the surface, in close proximity to the electron channel, in order to mitigate these thermal issues. Many thermal solutions have been considered including wafer thinning and bonding the β-Ga_2O_3

device to higher thermally conductive substrates (i.e., 4H-SiC or diamond).[8–12] Top-sided solutions, including heat-spreading layers, have been shown to be especially useful for lateral devices as the majority of the heat is generated near the surface of the wafer within the transistor active region.[5] Previously, we have demonstrated temperature reduction in the active region of a β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterojunction field effect transistor (HFET) with the incorporation of a sputtered-AlN heat-spreading layer.[13] Diamond has been extensively explored for heat spreading in GaN devices due to its high thermal conductivity[14–26] and its incorporation in a similar lateral HFET as in Ref. 18.

Nanocrystalline diamond (NCD) has been proposed to be an excellent candidate for a heat-spreading layer in wide bandgap devices due to its high thermal conductivity [200–1500 W (m K)$^{-1}$ depending on thickness], conformal growth across three-dimensional surfaces, small crystallite size (<100 nm), and low surface roughness (1–20 nm rms).[15] Chemical vapor deposition (CVD) of NCD can be performed by a variety of methods including hot-filament CVD (HF-CVD), microwave-plasma enhanced CVD (MP-CVD), DC glow discharge, and electron cyclotron resonance.[14,16] MP-CVD is a technique predominantly used for high quality, contamination-free diamond growth for single-crystalline, polycrystalline, nanocrystalline, and ultrananocrystalline diamond. The chemistry for NCD growth consists of methane (CH_4) precursor diluted in H_2, and the CH_4/H_2 ratio plays important role in defining the resulting properties of the CVD NCD films.[17] Previously, diamond grown by CVD has been incorporated into AlGaN/GaN devices either as a substrate (polycrystalline diamond) or as a top-side coating (NCD) and has resulted in improved device performance.[18–28]

Growth of NCD on β-Ga_2O_3 presents such challenges of etching the Ga_2O_3 in H_2 plasma, necessitating a reduced growth temperature and the use of a barrier dielectric such as SiN_x or SiO_2.[6,29] Reducing the growth temperature of NCD will result in a slower growth rate and typically leads to an increased concentration of sp^2-bonded carbon.[6] Low-temperature growth of diamond has been explored in the literature in the past.[30–33] Stiegler *et al.* showed crystalline CVD diamond growth at temperatures as low as 360 °C using a 2% CH_4/H_2 ratio and no additional oxygen in the plasma chemistry.[31] At higher CH_4/H_2 ratio, the NCD film transitioned into a "cauliflower" regime, typically characterized by a smaller crystallite size and voids in between grains.[34] As the growth temperature was reduced, the diamond Raman peak measured at 1333 cm^{-1} in samples became less distinguishable from the non-sp^3 background signal around 1500 cm^{-1}. Kriele *et al.* showed that non-sp^3 peaks (i.e., graphite and transpolyacetylene signals) can be significantly reduced by using a CH_4/H_2 ratio of up 1%.[40] Furthermore, it is well known that nanodiamond grain evolution can be assisted when a small amount of oxygen in the plasma etching smaller grains, allowing surviving columns the space to expand faster, result in increased grain size and thus improved diamond quality.[35–37] For example, Schmidt *et al.* performed detailed quadrupole mass spectrometry (QMS) gas-phase analysis during microwave-plasma CVD of diamond.[36] The improvement in the diamond quality, determined by the ratio of the diamond/non-diamond Raman peak intensities, was shown at an O_2 flow rate of about 1.8% (2 sccm O_2, 100 sccm H_2, and 6 sccm CH_4). The drawback of this growth process is that the transfer of carbon from the methane precursor must overcome the competing process of carbon etched by the oxygen, resulting in a reduced growth rate as shown in Fig. 10 in Schmidt's work.[36] This is significant when modifications of gas chemistry for the purpose of improving thermal conductivity, particularly for low growth temperature regimes, are proposed since NCD thermal conductivity is dependent on the total thickness and thus growth rate.[31] In this work, we grow NCD at 400 °C without the use of oxygen and preserve sp^3-bonding, as shown by Raman spectroscopy, by keeping the CH_4/H_2 ratio sufficiently low to preserve the transfer of carbon from the methane precursor into highly covalently bonded NCD. We demonstrate an NCD-capped β-$(Al_xGa_{1-x})_2O_3/$β-Ga_2O_3 heterostructure field-effect transistor (HFET) as a potential solution for top-side device-level thermal management for Ga_2O_3 power devices.

The fabricated NCD-capped β-Ga_2O_3 device cross section schematic is shown in Fig. 1(a). β-$(Al_xGa_{1-x})_2O_3/$β-Ga_2O_3 heterostructures were grown via ozone-assisted molecular beam epitaxy (O_3-MBE), which consists of a 125 nm thick unintentionally doped (UID) Ga_2O_3 layer, followed by a 28 nm thick $(Al_{0.19}Ga_{0.81})_2O_3$ barrier layer on an Fe-doped (010) Ga_2O_3 substrate.[38,39] The $(Al_{0.19}Ga_{0.81})_2O_3$ layer was delta-doped with Si ~3 nm above the interface. These layers were continuously grown in the MBE reactor to prevent unintentional Si from accumulating at the HFET interface. Net free carrier concentration of the heterostructure extracted by electrochemical C-V method is shown in Fig. 1(b). Ohmic source/drain contacts were formed using Si ion implantation with an activation anneal of 30 min at 925 °C in N_2 and e-beam evaporation of Ti/Au with a metallization anneal of 1 min at 470 °C in N_2.

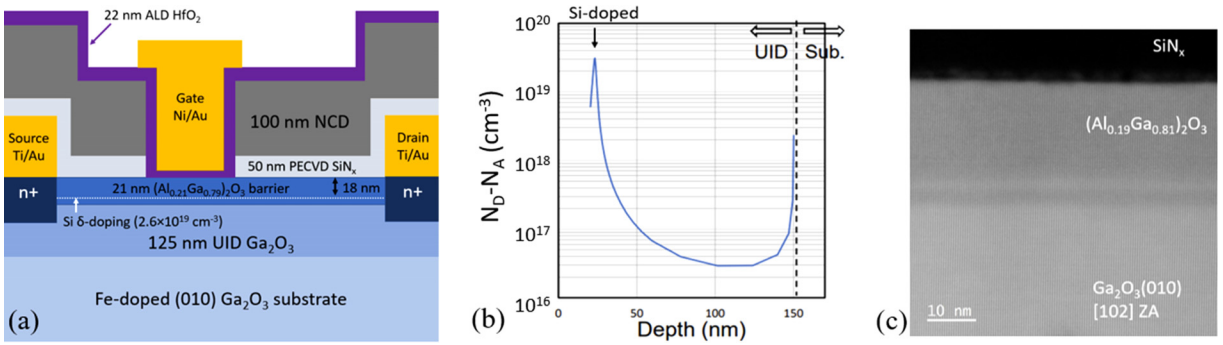

FIG. 1. (a) Cross-section schematic of the β-$(Al_xGa_{1-x})_2O_3/$β-Ga_2O_3 HFET with NCD heat-spreading layer. (b) Net doping concentration of the O_3-MBE grown heterostructure extracted by *C-V*. (c) HAADF-STEM of the β-$(Al_xGa_{1-x})_2O_3/$β-Ga_2O_3 heterostructure after NCD growth.

Prior to NCD growth, a ~50 nm thick SiN_x layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 400 °C to protect the Ga_2O_3 from damage caused by the H_2 plasma during the NCD growth.[6] The NCD layer was then grown by MP-CVD in a three-step process.[14,16] A seeding method using detonation nanodiamond powder creates the NCD nucleation sites.[15] The growth process started with seeded sample being placed into the growth chamber and pretreated at 100 °C in hydrogen atmosphere at 15 Torr for 1 h. NCD growth was then performed using a 1.5% CH_4/H_2 concentration at a temperature of 400 °C, pressure of 15 Torr, and power of 800 W for ~6 h, resulting in an NCD film thickness of ~100 nm.[17] Both SiN_x and NCD layers were continuous across the sample. Figure 1(c) shows a high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of the β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 heterostructures after NCD growth.

The SiN_x/NCD stack was then removed from the gate region and the source/drain probing pads. Because the NCD layer was thin and insulating, reference devices with the gate metal on top of the NCD ("Gate on NCD") were fabricated as well. An additional 100 nm thick PECVD SiN_x layer was deposited on the NCD film to act as a hard mask for the plasma dry etching process. O_2 plasma (ICP 1000 W, RF 100 W) and SF_6 (ICP 200 W, RF 50 W) were used to etch the NCD and SiN_x layers, respectively.[40] A 22 nm thick HfO_2 gate dielectric was deposited by atomic layer deposition (ALD), and finally, the gate contacts were formed by liftoff of a 20/200 nm thick e-beam evaporated Ni/Au stack. Figure 2(a) shows a secondary electron microscopy (SEM) image of a focused ion beam (FIB) cross section of the gate in an "MOS Gate" device. The various layers can be seen in the energy dispersive spectroscopy image of the source side of the gate in Fig. S1 in the supplementary material. The room temperature specific contact resistivity, mobility, sheet carrier concentration, and sheet resistance of the β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 heterostructures after NCD growth were measured to be $4.3 \times 10^{-4}\,\Omega \times \mathrm{cm}^2$, $54\,\mathrm{cm}^2/\mathrm{V{\cdot}s}$, $1.26 \times 10^{13}\,\mathrm{cm}^{-2}$, and 9.1 kΩ/□, respectively.

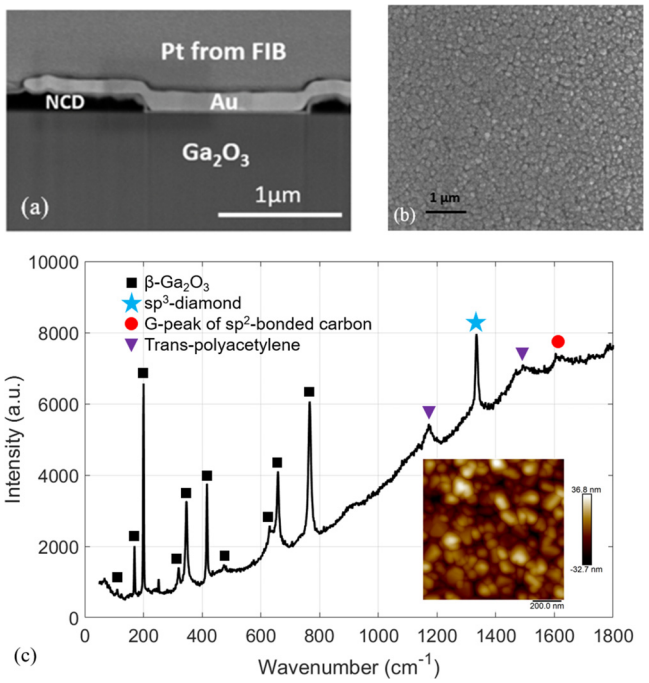

FIG. 2. (a) FIB SEM cross-sectional image of the gate region of the fabricated HFET. (b) SEM image of NCD grown on the β-Ga_2O_3 device. (c) Raman spectroscopy showing the diamond peak at ~1330 cm^{-1} indicating the sp^3-bonded carbon and inset showing an AFM image of a witness β-Ga_2O_3 sample. Grain size averages between 50 and 100 nm, and rms roughness is ~10 nm.

The SEM image of the NCD film grown on the delta-doped HFET sample in Fig. 2(b) shows a continuous NCD layer was grown at this reduced temperature of 400 °C without large voids in between the grains typically observed in cauliflower NCD films. From the atomic force microscope (AFM) image of a witness Ga_2O_3 sample [inset of Fig. 2(c)], the average grain size is estimated to range from 50 to 100 nm and an RMS roughness of ~10 nm was measured. Thicker NCD growth on Ga_2O_3 is planned in follow-up experiments in order to rigorously quantify NCD grain size and texture using x-ray diffraction (XRD), scanning transmission electron microscopy (STEM), precession electron diffraction (PED), and electron backscattering diffraction (EBSD) methods.[41–43] Raman spectroscopy of the NCD-capped HFET [Fig. 2(c)], a rapid NCD characterization technique, indicated a high quality NCD layer with sp^3-bonded carbon based on the sharp Raman mode at ~1332 cm^{-1} and suppressed trans-polyacetylene and G-peaks as a result of the low CH_4/H_2 ratio during NCD growth.[16,44,45]

Figures 3(a) and 3(b) show the DC transfer and output characteristic for the NCD-capped β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 HFET labeled "MOS gate." A low on-state $I_{D,max}$ of 4.7 mA/mm at a V_{DS} of 5 V, and threshold voltage (V_{th}) of 6 V were measured [Fig. 3(a)]. While no significant over-etching was observed in the cross-sectional SEM image of the "MOS gate," the SF_6-plasma may have impacted the $(Al_xGa_{1-x})_2O_3$ barrier within the gate region when removing the SiN_x interlayer. Output characteristics show lower I_D as well as significant increase in on-resistance possibly due to fluorination of the $(Al_xGa_{1-x})_2O_3$ barrier from exposure to the SF_6-plasma. Threshold voltage control due to fluoride-based plasma treatments has been extensively reported for GaN HEMTs.[46,47] Deposition of gate dielectric prior to SiN_x barrier could be one mitigating approach.[48] Ideally, it would be beneficial to increase diamond growth temperature in our future experiments. The higher growth temperature could be detrimental to the ALD gate dielectric properties, though, in this case.

In contrast, DC transfer and output measurements are shown in Figs. 3(c) and 3(d) for a reference "Gate on NCD" device still capped with NCD within the gate region. On-state I_D at the same V_{DS} of 5 V is 21 mA/mm [Fig. 3(c)], and output curves show I_D is over 20× higher compared to the "MOS Gate" device. The higher I_D for the "Gate on NCD" device can be attributed to the $(Al_xGa_{1-x})_2O_3$ barrier in the gate region not being exposed to the SF_6 plasma required to remove the SiN_x barrier layer. An uncapped reference HFET device characteristics from a sister sample on which SiN_x and NCD were not deposited are shown in Figs. 3(e) and 3(f).[13] The extracted V_{th} of the reference sample was −23 V. Although the current density was maintained in the "Gate on NCD" device compared to the reference device, the disadvantage of this structure with the additional layers in the gate region was the significant negative threshold voltage shift to a V_{th} of −40 V. The output characteristics in Fig. 3(d) do not show current saturation, which may be due to reduced 2DEG density control by the gate field at higher drain biases caused by the additional NCD and SiN_x layers over

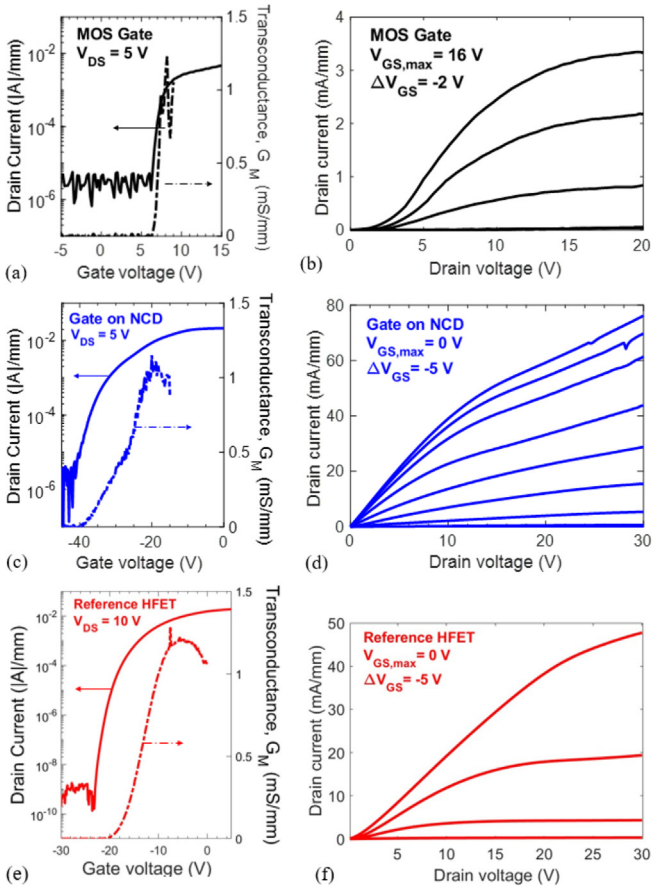

FIG. 3. (a) DC transfer and (b) output characteristics of the β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 HFET with the MOS gate. (c) DC transfer and (b) output characteristics of the β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 HFET with the gate on NCD. (e) DC transfer and (f) output characteristics of the β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 reference HFET. All devices have the following geometry: $L_{GS} = 2.5\ \mu$m, $L_{GD} = 10\ \mu$m, and $W_G = 75\ \mu$m.

the channel. The NCD/SiN_x stack etch process in the gate region will need to be optimized in order to achieve the higher drain current while maintaining a reasonable threshold voltage.

Both "MOS gate" and "Gate on NCD" devices do show a higher off-state leakage current compared to the reference device. After the NCD growth at 400 °C, we may be activating an additional conduction path through the Si peak at the Ga_2O_3 buffer/substrate interface as shown in Fig. 1(b); this could be mitigated in future iterations by growing a thicker Ga_2O_3 buffer layer. Another possibility could be hydrogen from the CH_4/H_2 plasma during NCD CVD growth incorporating into the device layers and increasing the conductivity, as hydrogen interstitials have been reported to act as a shallow donor in β-Ga_2O_3.[49] A significant drop in Hall mobility was observed from 83 to 54 cm^2/V·s, measured before and after NCD growth, respectively. The higher off-state leakage and reduction in Hall mobility may indicate the need to continue using a lower NCD growth temperature (e.g., 400 °C) to avoid further device degradation. Additional electrical data, including gate leakage, isolation currents, and Hall measurements, are provided in the supplementary material.

Thermal measurements were performed using a TMX Scientific T°Imager (532 nm, 100× objective); the power dissipated was monitored using an oscilloscope, and the base temperature was maintained at 20 °C. A measurement delay of 5 ms was employed to allow the device to reach a steady-state thermal condition before measuring the operating temperature rise.[12] Figure 4(a) shows the temperature rise across the NCD-capped HFET compared to the reference uncapped HFET at a power density of ∼1.6 W/mm ($V_{GS} = 0$ V) with the inset showing the thermoreflectance image of the NCD-capped HFET. Figure 4(b) shows the average temperature rise at the gate as a function of power density where the slope corresponds to the device thermal resistance. A 42% reduction in the thermal resistance at the gate electrode was observed with the incorporation of the NCD heat-spreading layer when compared to a reference uncapped HFET.[13]

To evaluate the thermal conductivity of the NCD film and thermal boundary resistance (TBR) of the associated interfaces, time domain thermoreflectance (TDTR) was used. TDTR is a well-established optical pump-probe method for measuring thermal

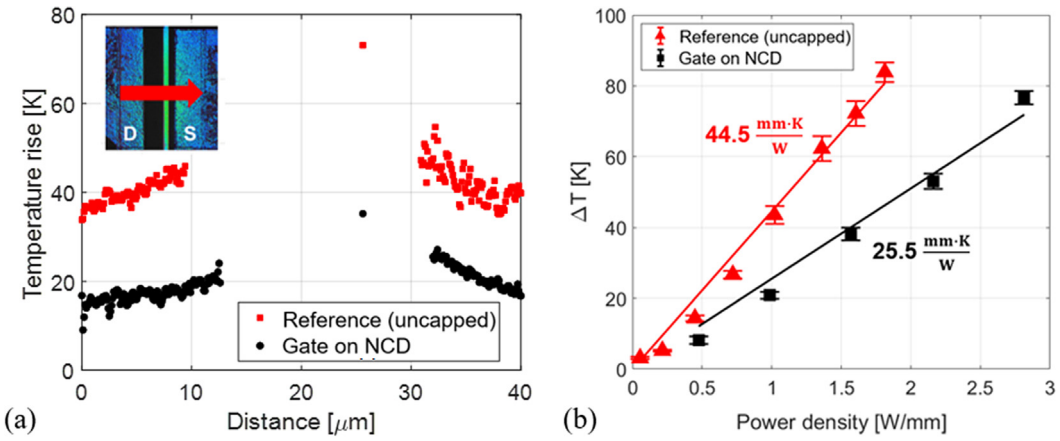

FIG. 4. (a) Temperature rise across the NCD-capped HFET compared to a reference HFET at 1.6 W/mm ($V_{GS} = 0$ V). Inset shows the thermoreflectance image of the NCD-capped HFET at a power density of 1.6 W/mm. (b) Average temperature rise of the gate vs power density for NCD-capped and reference (uncapped) HFETs with the extracted thermal resistances.

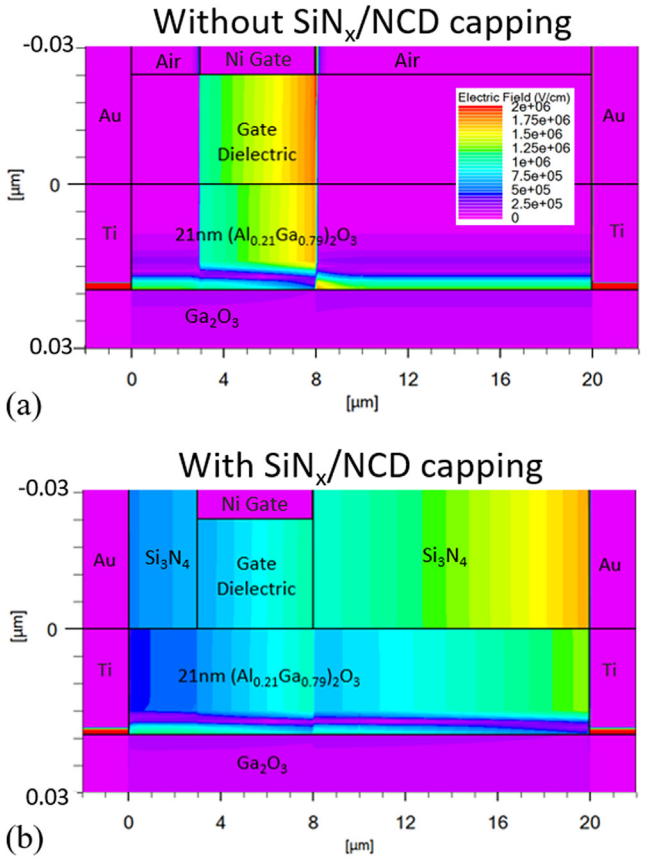

FIG. 5. (a) Electric field (E) simulations ($V_{DS} = 8$ V, $V_{GS} = 0$ V) for (a) the reference device and (b) the SiN_x/NCD-capped device.

properties of thin films and interfaces.[50,51] For sample preparation, a thin film metal transducer is deposited onto the surface of the sample. In this study, the transducer was 80 nm of Al deposited via e-beam evaporation. In the current TDTR experimental setup, a single laser (Ti:sapphire, 800 nm) is used to both periodically heat the sample surface (pump beam path) and measure the change in reflectivity of the metal transducer (probe beam path). The incident laser passes through a polarizing beam splitter to divide the laser into the pump and probe beam paths. The frequency of the pump beam is then doubled to 400 nm for surface heating, and the probe beam passes through a mechanical delay stage to measure the thermal response (change in reflectivity) with picosecond temporal resolution. A diffusive heat conduction model is subsequently used to fit thermal conductivity and TBR.[50,51] For the Al/NCD/SiN_x/Ga_2O_3 sample, a sensitivity analysis revealed extremely low sensitivity to the thermal conductivity of the NCD film, and the measurement sensitivity was dominated by the SiN_x interlayer and the NCD/SiN_x/Ga_2O_3 interfaces. This indicates that the thermal resistance of the SiN_x interlayer and NCD/SiN_x/Ga_2O_3 interfaces is significantly larger than that of the NCD film. As such, the measured thermal resistance of 51 m^2·K/GW comprised the NCD film, SiN_x interlayer, and NCD/SiN_x/Ga_2O_3 interfaces. Additional information on the sensitivity analysis and data fitting is available in the supplementary material. Significantly thicker NCD layers are needed for accurate thermal conductivity analysis of low-temperature NCD.

In addition to thermal benefits, the higher dielectric relative permittivity compared to air of the NCD and the SiN_x layers, 5.5[44] and ~10, respectively, leads to improved field management within the $(Al_xGa_{1-x})_2O_3$ layer. Silvaco simulation results show spreading of the electric field (E) within the $(Al_xGa_{1-x})_2O_3$ layer due to the implementation of the SiN_x/NCD film stack [Fig. 5(b)] compared to the reference uncapped device [Fig. 5(a)]. The devices in these simulations were biased at $V_{DS} = 8$ V and $V_{GS} = 0$ V. This electrothermal management technique will become more effective with optimization of the NCD layer, including using a higher deposition temperature, growing a thicker NCD layer, and reducing the thickness of the SiN_x interlayer.[44]

Here, we report the results of a nanocrystalline-diamond capped β-Ga_2O_3 device and the resulting reduction in device operating temperature. A heat-spreading NCD layer of 100 nm was grown using microwave plasma enhanced CVD on a partially processed β-$(Al_xGa_{1-x})_2O_3$/β-Ga_2O_3 heterostructure device. The 50 nm SiN_x interlayer was crucial to avoid hydrogen plasma damaging the β-Ga_2O_3. A significant reduction in drain current was observed when removing the NCD/SiN_x stack from the gate region with plasma etching, but drain current was maintained when the gate was formed on top of the NCD/SiN_x stack. Incorporation of the NCD-capping layer resulted in a 42% reduction of thermal resistance at the gate, which shows the promise of this technique as a thermal management solution for β-Ga_2O_3-based power devices. These results outline two paths forward for future works. On the one hand, we could continue using a low (400–500 °C) NCD growth temperature and form the gate prior to NCD growth; this would avoid the need for plasma etching in the active region. The other path forward includes increasing the growth temperature of the NCD, which increases the growth rate; this would allow us to grow thicker NCD films prior to gate deposition and optimize its thermal properties. With higher growth temperatures, we would need to improve the etch of the NCD/protective layer (SiN_x) stack and possibly investigate other protective layers that would better impede hydrogen incorporation into the Ga_2O_3.

See the supplementary material for additional information, including energy dispersive spectroscopy image of the NCD-capped Ga_2O_3 device (Fig. S1), additional electrical data (Figs. S2–S4, Table S1), TDTR setup, sensitivity analysis, and analysis (Table S2, Figs. S5 and S6), and full schematics of the Silvaco simulations (Fig. S7).

H.N.M. and J.S.L gratefully acknowledge support by the NRC postdoctoral fellowship program. Research at the NRL was supported by the ONR. Research at NCT, Inc., was partially supported by ONR Global.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Hannah N. Masten: Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – original draft (equal); Writing – review & editing (equal). **James Spencer Lundh:** Data curation (equal);

Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Tatyana I. Feygelson:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Kohei Sasaki:** Data curation (equal); Methodology (equal); Resources (equal). **Zhe Cheng:** Data curation (equal); Formal analysis (equal); Writing – review & editing (equal). **Joseph A. Spencer:** Data curation (equal); Investigation (equal). **Pai-Ying Liao:** Resources (equal). **Jennifer K. Hite:** Data curation (equal); Investigation (equal). **Daniel J. Pennachio:** Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Alan G. Jacobs:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal). **Michael A. Mastro:** Data curation (equal); Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Boris N. Feigelson:** Conceptualization (equal); Methodology (equal). **Akito Kuramata:** Methodology (equal); Resources (equal). **Peide Ye:** Resources (equal). **Samuel Graham:** Conceptualization (equal); Investigation (equal); Resources (equal); Writing – review & editing (equal). **Bradford B. Pate:** Conceptualization (equal); Investigation (equal); Methodology (equal). **Karl D. Hobart:** Conceptualization (equal); Funding acquisition (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **Travis J. Anderson:** Conceptualization (equal); Funding acquisition (equal); Methodology (equal). **Marko J. Tadjer:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Development of gallium oxide power devices," Phys. Status Solidi A **211**(1), 21–26 (2014).

[2]M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, "Recent progress in Ga_2O_3 power devices," Semicond. Sci. Technol. **31**(3), 034001 (2016).

[3]A. J. Green, J. Speck, G. Xing, P. Moens, F. Allerstam, K. Gumaelius, T. Neyer, A. Arias-Purdue, V. Mehrotra, A. Kuramata, K. Sasaki, S. Watanabe, K. Koshi, J. Blevins, O. Bierwagen, S. Krishnamoorthy, K. Leedy, A. R. Arehart, A. T. Neal *et al.*, "β-Gallium oxide power electronics," APL Mater. **10**(2), 029201 (2022).

[4]Z. Cheng, L. Yates, J. Shi, M. J. Tadjer, K. D. Hobart, and S. Graham, "Thermal conductance across β-Ga_2O_3-diamond van der Waals heterogeneous interfaces," APL Mater. **7**(3), 031118 (2019).

[5]K. D. Chabak, K. D. Leedy, A. J. Green, S. Mou, A. T. Neal, T. Asel, E. R. Heller, N. S. Hendricks, K. Liddy, A. Crespo, N. C. Miller, M. T. Lindquist, N. A. Moser, R. C. Fitch, D. E. Walker, D. L. Dorsey, and G. H. Jessen, "Lateral β-Ga_2O_3 field effect transistors," Semicond. Sci. Technol. **35**(1), 013002 (2020).

[6]M. Malakoutian, Y. Song, C. Yuan, C. Ren, J. S. Lundh, R. M. Lavelle, J. E. Brown, D. W. Snyder, S. Graham, S. Choi, and S. Chowdhury, "Polycrystalline diamond growth on β-Ga_2O_3 for thermal management," Appl. Phys. Express **14**(5), 055502 (2021).

[7]R. H. Montgomery, Y. Zhang, C. Yuan, S. Kim, J. Shi, T. Itoh, A. Mauze, S. Kumar, J. Speck, and S. Graham, "Thermal management strategies for gallium oxide vertical trench-fin MOSFETs," J. Appl. Phys. **129**(8), 085301 (2021).

[8]Y. Song, A. Bhattacharyya, A. Karim, D. Shoemaker, H. L. Huang, S. Roy, C. McGray, J. H. Leach, J. Hwang, S. Krishnamoorthy, and S. Choi, "Ultra-wide band gap Ga_2O_3-on-SiC MOSFETs," ACS Appl. Mater. Interfaces **15**(5), 7137–7147 (2023).

[9]Y. Song, D. Shoemaker, J. H. Leach, C. McGray, H. L. Huang, A. Bhattacharyya, Y. Zhang, C. U. Gonzalez-Valle, T. Hess, S. Zhukovsky, K. Ferri, R. M. Lavelle, C. Perez, D. W. Snyder, J. P. Maria, B. Ramos-Alvarado, X. Wang, S. Krishnamoorthy, J. Hwang *et al.*, "Ga_2O_3-on-SiC composite wafer for thermal management of ultrawide bandgap electronics," ACS Appl. Mater. Interfaces **13**(34), 40817–40829 (2021).

[10]W. Xu, Y. Wang, T. You, X. Ou, G. Han, H. Hu, S. Zhang, F. Mu, T. Suga, Y. Zhang, Y. Hao, and X. Wang, "First demonstration of waferscale heterogeneous integration of Ga_2O_3 MOSFETs on SiC and Si substrates by ion-cutting process," in *IEEE International Electron Devices Meeting* (IEEE, 2019).

[11]Y. Wang, W. Xu, G. Han, T. You, F. Mu, H. Hu, Y. Liu, X. Zhang, H. Huang, T. Suga, X. Ou, X. Ma, and Y. Hao, "Channel properties of Ga_2O_3-on-SiC MOSFETs," IEEE Trans. Electron Devices **68**(3), 1185–1189 (2021).

[12]S. H. Kim, D. Shoemaker, A. J. Green, K. D. Chabak, K. J. Liddy, S. Graham, and S. Choi, "Transient thermal management of a β-Ga_2O_3 MOSFET using a double-side diamond cooling approach," IEEE Trans. Electron Devices **70**(4), 1628 (2023).

[13]J. S. Lundh, H. N. Masten, K. Sasaki, A. G. Jacobs, Z. Cheng, J. Spencer, L. Chen, J. Gallagher, A. D. Koehler, K. Konishi, S. Graham, A. Kuramata, K. D. Hobart, and M. J. Tadjer, "AlN-capped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure field-effect transistors for near-junction thermal management of next generation power devices," in *Device Research Conference - Conference Digest, DRC* (IEEE, 2022), Vol. 2022.

[14]O. A. Williams, "Nanocrystalline diamond," Diamond Related Mater. **20**(5–6), 621–640 (2011).

[15]T. I. Feygelson, M. J. Tadjer, K. D. Hobart, T. J. Anderson, and B. B. Pate, "Reduced-stress nanocrystalline diamond films for heat spreading in electronic devices," in *Thermal Management of Gallium Nitride Electronics* (Elsevier, 2022), pp. 275–294.

[16]J. E. Butler and A. V. Sumant, "The CVD of nanodiamond materials," Chem. Vap. Deposition **14**(7–8), 145–160 (2008).

[17]J. Philip, P. Hess, T. Feygelson, J. E. Butler, S. Chattopadhyay, K. H. Chen, and L. C. Chen, "Elastic, mechanical, and thermal properties of nanocrystalline diamond films," J. Appl. Phys. **93**(4), 2164–2171 (2003).

[18]F. Ejeckam, D. Francis, F. Faili, D. Twitchen, B. Bolliger, D. Babic, and J. Felbinger, "S2-T1: GaN-on-diamond: A brief history," in *Lester Eastman Conference on High Performance Devices (LEC)* (IEEE, 2014).

[19]M. J. Tadjer, T. J. Anderson, M. G. Ancona, P. E. Raad, P. Komarov, T. Bai, J. C. Gallagher, A. D. Koehler, M. S. Goorsky, D. A. Francis, K. D. Hobart, and F. J. Kub, "GaN-On-diamond HEMT technology with $T_{AVG} = 176$ C at $P_{DC,max} = 56$ W/mm measured by transient thermoreflectance imaging," IEEE Electron Device Lett. **40**(6), 881–884 (2019).

[20]M. J. Tadjer, T. J. Anderson, K. D. Hobart, T. I. Feygelson, J. D. Caldwell, C. R. Eddy, F. J. Kub, J. E. Butler, B. Pate, and J. Melngailis, "Reduced self-heating in AlGaN/GaN HEMTs using nanocrystalline diamond heat-spreading films," IEEE Electron Device Lett. **33**(1), 23–25 (2012).

[21]M. J. Tadjer and T. J. Anderson, *Thermal Management of Gallium Nitride Electronics* (Elsevier Science, 2022), pp. 1–477.

[22]M. Seelmann-Eggebert, P. Meisen, F. Schaudel, P. Koidl, A. Vescan, and H. Leier, "Heat-spreading diamond films for GaN-based high-power transistor devices," Diamond Related Mater. **10**(3–7), 744–749 (2001).

[23]G. H. Jessen, J. K. Gillespie, G. D. Via, A. Crespo, D. Langley, G. J. Wasserbauer, F. Faili, D. Francis, D. Babic, F. Ejeckam, and S. Guo, "AlGaN/GaN HEMT on diamond technology demonstration," in *IEEE Compound Semiconductor Integrated Circuit Symposium* (IEEE, 2006).

[24]D. Francis, F. Faili, D. Babić, F. Ejeckam, A. Nurmikko, and H. Maris, "Formation and characterization of 4-inch GaN-on-diamond substrates," Diamond Related Mater. **19**, 229–233 (2009).

[25]P. C. Chao, K. Chu, C. Creamer, J. Diaz, T. Yurovchak, M. Shur, R. Kallaher, C. McGray, G. D. Via, and J. D. Blevins, "Low-temperature bonded GaN-on-diamond HEMTs with 11 W/mm output power at 10 GHz," IEEE Trans Electron Devices **62**(11), 3658–3664 (2015).

[26]M. Alomari, M. Dipalo, S. Rossi, M.-A. Diforte-Poisson, S. Delage, J.-F. Carlin, N. Grandjean, C. Gaquiere, L. Toth, B. Pecz, and E. Kohn, "Diamond

overgrown InAlN/GaN HEMT," Diamond Related Mater. **20**(4), 604–608 (2011).
[27]F. Mu and T. Suga, "Room temperature GaN-diamond bonding for high-power GaN-on-diamond devices," Scr. Mater. **150**, 148–151 (2018).
[28]T. J. Anderson, K. D. Hobart, M. J. Tadjer, A. D. Koehler, E. A. Imhoff, J. K. Hite, T. I. Feygelson, B. B. Pate, C. R. Eddy, and F. J. Kub, "Nanocrystalline diamond integration with III-nitride HEMTs," ECS J. Solid State Sci. Technol. **6**(2), Q3036–Q3039 (2017).
[29]S. Mandal, K. Arts, H. C. M. Knoops, J. A. Cuenca, G. M. Klemencic, and O. A. Williams, "Surface zeta potential and diamond growth on gallium oxide single crystal," Carbon **181**, 79–86 (2021).
[30]V. Goyal, A. V. Sumant, D. Teweldebrhan, and A. A. Balandin, "Direct low-temperature integration of nanocrystalline diamond with GaN substrates for improved thermal management of high-power electronics," Adv. Funct. Mater. **22**(7), 1525–1530 (2012).
[31]M. Malakoutian, X. Zheng, K. Woo, R. Soman, A. Kasperovich, J. Pomeroy, M. Kuball, and S. Chowdhury, "Low thermal budget growth of near-isotropic diamond grains for heat spreading in semiconductor devices," Adv. Funct. Mater. **32**(47), 2208997 (2022).
[32]J. Stiegler, T. Lang, M. Nygåtrd-Ferguson, Y. Von Kaenel, and E. Blank, "Low temperature limits of diamond film growth by microwave plasma-assisted CVD," Diamond Related Mater. **5**(3–5), 226–230 (1996).
[33]Y. Muranaka, H. Yamashita, and H. Miyadera, "Characterization of diamond films synthesized in the microwave plasmas of CO/H_2 and $CO/O_2/H_2$ systems at low temperatures (403–1023 K)," J. Appl. Phys. **69**(12), 8145–8153 (1991).
[34]J. Millán-Barba, A. Taylor, H. Bakkali, R. Alcantara, F. Lloret, R. G. de Villoria, M. Dominguez, V. Mortet, M. Gutiérrez, and D. Araújo, "Low temperature growth of nanocrystalline diamond: Insight thermal property," Diamond Related Mater. **137**, 110070 (2023).
[35]T. Kawato and K. Kondo, "Effects of oxygen on CVD diamond synthesis," Jpn. J. Appl. Phys., Part 1 **26**(9R), 1429 (1987).
[36]I. Schmidt, C. Benndorf, and P. Joeris, "Gas phase composition and film properties of hot filament diamond synthesis from CH_4-H_2-O_2 gas mixtures," Diamond Related Mater. **4**(5–6), 725–729 (1995).
[37]F. M. Cerio, W. A. Weimer, and C. E. Johnson, "Diamond growth using carbon monoxide as a carbon source," J. Mater. Res. **7**(5), 1195–1203 (1992).
[38]M. J. Tadjer, K. Sasaki, D. Wakimoto, T. J. Anderson, M. A. Mastro, J. C. Gallagher, A. G. Jacobs, A. L. Mock, A. D. Koehler, M. Ebrish, K. D. Hobart, and A. Kuramata, "Delta-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure field-effect transistors by ozone molecular beam epitaxy," J. Vac. Sci. Technol. A **39**(3), 033402 (2021).
[39]K. Sasaki, A. Kuramata, T. Masui, E. G. Víllora, K. Shimamura, and S. Yamakoshi, "Device-quality β-Ga_2O_3 epitaxial films fabricated by ozone molecular beam epitaxy," Appl. Phys. Express **5**(3), 035502 (2012).
[40]H. N. Masten, J. S. Lundh, J. A. Spencer, T. Feygelson, J. Hite, D. Pennachio, A. G. Jacobs, B. Feygelson, K. Sasaki, A. Kuramata, P.-Y. Liao, P. Ye, B. Pate, K. D. Hobart, T. J. Anderson, and M. J. Tadjer, "11.4 nanocrystalline diamond-capped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterostructure field-effect transistor," in *CS Mantech* (CS Mantech, 2023).
[41]P. Scherrer, "Nachr Ges wiss goettingen," Math. Phys. **2**, 98–100 (1918).
[42]T. Bai, Y. Wang, T. I. Feygelson, M. J. Tadjer, K. D. Hobart, N. J. Hines, L. Yates, S. Graham, J. Anaya, M. Kuball, and M. S. Goorsky, "Diamond seed size and the impact on chemical vapor deposition diamond thin film properties," ECS J. Solid State Sci. Technol. **9**(5), 053002 (2020).
[43]J. Anaya, T. Bai, Y. Wang, C. Li, M. Goorsky, T. L. Bougher, L. Yates, Z. Cheng, S. Graham, K. D. Hobart, T. I. Feygelson, M. J. Tadjer, T. J. Anderson, B. B. Pate, and M. Kuball, "Simultaneous determination of the lattice thermal conductivity and grain/grain thermal resistance in polycrystalline diamond," Acta Mater. **139**, 215–225 (2017).
[44]O. A. Williams and M. Nesládek, "Growth and properties of nanocrystalline diamond films," Phys. Status Solidi A **203**(13), 3375–3386 (2006).
[45]A. Kriele, O. A. Williams, M. Wolfer, D. Brink, W. Müller-Sebert, and C. E. Nebel, "Tuneable optical lenses from diamond thin films," Appl. Phys. Lett. **95**(3), 031905 (2009).
[46]Y. Cai, Y. Zhou, K. M. Lau, and K. J. Chen, "Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based plasma treatment: From depletion mode to enhancement mode," IEEE Trans. Electron Devices **53**(9), 2207–2214 (2006).
[47]Y. Cai, Y. Zhou, K. J. Chen, and K. M. Lau, "High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment," IEEE Electron Device Lett. **26**(7), 435–437 (2005).
[48]K. Tetzner, E. Bahat Treidel, O. Hilt, A. Popp, S. Bin Anooz, G. Wagner, A. Thies, K. Ickert, H. Gargouri, and J. Wurfl, "Lateral 1.8 kV β-Ga_2O_3 MOSFET With 155 MW/cm^2 power figure of merit," IEEE Electron Device Lett. **40**(9), 1503–1506 (2019).
[49]J. B. Varley, J. R. Weber, A. Janotti, and C. G. Van De Walle, "Oxygen vacancies and donor impurities in β-Ga_2O_3," Appl. Phys. Lett. **97**(14), 142106 (2010).
[50]L. Yates, Z. Cheng, T. Bai, K. Hobart, M. Tadjer, T. I. Feygelson, B. B. Pate, M. Goorsky, and S. Graham, "Simultaneous evaluation of heat capacity and in-plane thermal conductivity of nanocrystalline diamond thin films," Nanoscale Microscale Thermophys. Eng. **25**(3–4), 166–178 (2021).
[51]T. L. Bougher, L. Yates, C. F. Lo, W. Johnson, S. Graham, and B. A. Cola, "Thermal boundary resistance in GaN films measured by time domain thermoreflectance with robust Monte Carlo uncertainty estimation," Nanoscale Microscale Thermophys. Eng. **20**(1), 22–32 (2016).